AMENDMENTS TO THE CLAIMS:

Please amend claims 1 and 3-6, and add new claims 7-20 as follows. The following listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (Currently Amended). A method of processing a signal using a digital signal processor having a given word length, the method comprising: ~~the step of~~

pre-processing said signal using a pre-processor which reduces the word length and performs an operation which is invariant with respect to ~~the~~ a process being performed by the digital signal processor;

transforming the pre-processed signal into frequency coefficients; and

normalizing the frequency coefficients directly after the transformation of the pre-processed signal into frequency coefficients whereby quantization noise is thereby reduced in said process being performed by the digital signal processor.

Claim 2 (Original). A method as claimed in claim 1, wherein said process being performed by the digital signal processor is

watermark detection, and the pre-processor is a high-pass filter.

Claim 3 (Currently Amended). A method of processing a signal received in the form of signal samples having a range of sample values, the method comprising: ~~the steps of~~

filtering the signal to reduce the range of signal sample values in a given band of non-interest, and thereafter

digitally processing the filtered signal using integer arithmetic, said step of digitally processing the filtered signal including transforming the filtered signal into frequency coefficients using an integer transform circuit.

Claim 4 (Currently Amended). A digital signal processor comprising: [[-]]

input means for receiving a signal in the form of integer signal samples having a range of sample values; [[-]]

filtering means ~~to reduce~~ for receiving the signal from said input means and reducing the range of signal sample values in a band of non-interest to form a filtered signal; [[-]] and

a digital signal processing circuit for receiving the filtered signal from said filtering means and digitally processing the filtered signal using integer arithmetic, said digital signal processing circuit comprising an integer transform circuit that transforms the filtered signal into frequency

coefficients.

Claim 5 (Currently amended). A processor as claimed in claim 4, wherein said ~~digital processing circuit comprises a~~ transform circuit ~~for transforming the signal into frequency coefficients~~ is an integer Fast Fourier Transform circuit.

Claim 6 (Currently Amended). A ~~processor~~ method as claimed in claim 3, wherein said ~~correlation circuit includes a Fourier transform circuit for computing said correlation for a plurality of shifts between said signal and said predetermined watermark pattern~~ integer transform circuit is a Fast Fourier Transform circuit.

Claim 7 (New). A method as claimed in claim 1, wherein the pre-processed signal is transformed into frequency coefficients by a Fast Fourier Transform circuit.

Claim 8 (New). A method as claimed in claim 1, wherein the pre-processed signal is transformed into frequency coefficients by an integer Fast Fourier Transform circuit.

Claim 9 (New). A method as claimed in claim 1, wherein the pre-processed signal is transformed into frequency coefficients

by a two-dimensional Fast Fourier Transform circuit.

Claim 10 (New). A method as claimed in claim 1, wherein the frequency coefficients are normalized by a symmetrical phase only matched filtering unit that extracts the phase of the frequency coefficients.

Claim 11 (New). A method as claimed in claim 1, wherein the pre-processor is a filter which reduces the dynamic range of said signal.

Claim 12 (New). A method as claimed in claim 1, wherein the digital signal processor uses integer arithmetic.

Claim 13 (New). A method as claimed in claim 1, wherein said signal is pre-processed by the pre-processor prior to the first signal processing step being performed by the digital signal processor.

Claim 14 (New). A method as claimed in claim 3, wherein the signal samples constitute a first pattern, further comprising:

filtering an additional signal received in the form of a second pattern of signal samples having a range of sample values;

digitally processing the filtered additional signal using

integer arithmetic, said step of digitally processing the filtered additional signal including transforming the filtered additional signal into frequency coefficients using an integer transform circuit; and

correlating between the first and second patterns by performing multiplication in the frequency domain.

Claim 15 (New). A method as claimed in claim 14, further comprising:

applying an inverse transform circuit to the multiplied frequencies; and

post-filtering the multiplied frequencies prior to application of the inverse transform circuit.

Claim 16 (New). A method as claimed in claim 15, wherein the second pattern is fixed, further comprising combining the post-filtering of the multiplied frequencies with the filtering of the additional signal and the transformation of the additional signal into frequency coefficients.

Claim 17 (New). A method as claimed in claim 3, wherein said step of digitally processing the filtered signal further comprises normalizing the frequency coefficients directly after the transformation of the pre-processed signal into frequency

coefficients.

Claim 18 (New). A method as claimed in claim 17, wherein the frequency coefficients are normalized by a symmetrical phase only matched filtering unit which extracts the phase of the frequency coefficients.

Claim 19 (New). A processor as claimed in claim 4, wherein said digital signal processing circuit further comprises a normalization circuit for normalizing the transformed pre-processed signal.

Claim 20 (New). A processor as claimed in claim 19,wherein said normalization circuit comprises a symmetrical phase only matched filtering component which extracts the phase of the frequency coefficients.